Farimah Farahmandi

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Research Interests

Design Automation of SoCs and Energy-efficient Systems, Post-silicon Validation and Debug, Approximate Computing, Internet-of-Things, and Formal Verification of SoCs.

Education

University of Florida, Gainesville, FL
Doctor of Philosophy in Computer Engineering — August 2013 – August 2018
Thesis: Formal Verification of Hardware Security and Trust

University of Tehran, Tehran, Iran
Master of Science in Computer Engineering — September 2010 – August 2013
Thesis: Verification of Arithmetic Circuits Based on Gröbner Basis Method

University Tehran, Tehran, Iran
Bachelor of Science in Computer Engineering — September 2006 – September 2010
Thesis: Reconfigurable Functional Unit for Embedded Processor Based on PSO Algorithm

Honors and Awards

1. Ph.D. Forum at Design Automation Conference, ACM SIGDA, San Francisco, CA, June 2018.
2. Gartner Group Info Tech Scholarship, CISE Department, University of Florida, March 2017.
3. ACM Capital Region Celebration of Women In Computing Scholarship, Washington, D.C., USA, February 2017.
4. Best paper award nomination, Asia and South Pacific Design Automation Conference, Tokyo, Japan, January 2017.
5. IEEE System Validation and Debug Technology Committee Student Research Award, January 2017.
6. CRA-W (Computing Research Association-Women) Grad Cohort Scholarship, San Diego, CA, April 2016.
7. DAC Richard Newton Young Student Fellowship Award, San Francisco, June 2015.
8. Selected as an exceptional talent and admitted to graduate studies (M. Sc. program) without participating in nationwide university entrance exam, University of Tehran, Tehran, Iran, September 2010.
9. Ranked top 0.1% nationwide matriculation exam - 493^{th} among 500,000, September 2006.

Professional Experience

Assistant Professor at the University of Florida Gainesville, FL	Spring 2018 – Present
Postdoc Researcher at the University of Florida Gainesville, FL	Summer 2018 – Fall 2018
Graduate Research Assistant at the University of Florida Gainesville, FL	Summer 2014 – Summer 2018
Internship at Cisco Systems**,** RTP, NC	Summer 2016
Graduate Research Assistant at the University of Tehran**,** Tehran, Iran	Fall 2011 – Summer 2013
Undergraduate Research Assistant at the University of Tehran**,** Tehran, Iran	Spring 2010 – September 2010

Publications

Books

1. **F. Farahmandi**, Yuanwen Huang, and P. Mishra, "Validation and Verification of Hardware Security", Springer, February 2019 (in preparation).
2. P. Mishra and **F. Farahmandi** (Editors), Post-Silicon Validation and Debug, ISBN: 978-3-319-98115-4, Springer, 2018.

Book Chapters

1. **F. Farahmandi** and P. Mishra, "Post-Silicon SoC Validation Challenges," Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
2. **F. Farahmandi** and P. Mishra, "Observability-aware Post-Silicon Test Generation," Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.

3. **F. Farahmandi** and P. Mishra, "The Future of Post-Silicon Debug," Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
4. **F. Farahmandi** and P. Mishra, "Utilization of Debug Infrastructure for Post-Silicon Coverage Analysis," Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
5. A. Ahmed, **F. Farahmandi**, Y. Iskander and Prabhat Mishra, "Security and Trust Verification of IoT SoCs," Security and Fault tolerance in Internet of Things, S. Chakraborty and J. Mathew (editors), Springer, 2019 (In print).
6. **F. Farahmandi** and Prabhat Mishra, "Validation of IP Security and Trust," Hardware IP Security and Trust, P. Mishra, S. Bhunia and M. Tehranipoor (editors), Springer, 2017.
7. **F. Farahmandi**, Yuanwen Huang and Prabhat Mishra, "Formal Approaches to Hardware Trust Verification," The Hardware Trojan War: Attacks, Myths, and Defenses, S. Bhunia and M. Tehranipoor (editors), Springer, 2017.

Peer-Reviewed Journal Articles

1. **F. Farahmandi** and P. Mishra, "Automated Test Generation for Debugging Multiple Unknown Bugs in Arithmetic Circuits," accepted in *IEEE Transaction on Computers (TC)*, 2018.
2. A. Nahiyan, **F. Farahmandi**, D. Forte, P. Mishra and M. Tehranipoor, "Security-aware FSM Design Flow for Mitigating Vulnerabilities to Fault Injection Attacks," accepted in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2018.
3. **F. Farahmandi** and B. Alizadeh, "Gröebner basis based Formal Verification of Large Arithmetic Circuits using Gaussian Elimination and Cone-based Polynomial Extraction," in *Microprocessors and Microsystems - Embedded Hardware Design*, vol. 39, no. 2, pages 83-96, 2015.
   —Under Review
4. **F. Farahmandi**, R. Morad, A. Ziv, Z. Nevo and P. Mishra, "Post-Silicon Functional Coverage Analysis utilizing Design-for-Debug Infrastructure," to be submitted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2019.

Published Peer-Reviewed Conference Papers

1. A. Ahmed, **F. Farahmandi**, J. Cruz, Y. Iskander and P. Mishra, "Scalable Hardware Trojan Detection by Interleaving Concrete Simulation and Symbolic Execution," accepted in *IEEE International Test Conference (ITC)*, Phoenix, AZ, October 28 - November 2, 2018.
2. A. Ahmed, **F. Farahmandi** and P. Mishra, "Directed Test Generation using Concolic Testing on RTL models," in *Design Automation and Test in Europe (DATE)*, pages 1538-1543, Dresden, Germany, March 19-23, 2018.
3. J. Cruz, **F. Farahmandi**, A. Ahmed, and P. Mishra, "Hardware Trojan Detection using ATPG and Model Checking," in *International Conference on VLSI Design (VLSI Design)*, pages 91-96, Pune, India, January 6 - 10, 2018.
4. **F. Farahmandi**, and P. Mishra, "Automated Debugging of Arithmetic Circuits using Incremental Gröbner Basis Reduction," in *IEEE International Conference on Computer Design (ICCD)*, pages 193-200, Boston, United States, November 5 - 8, 2017.
5. **F. Farahmandi**, R. Morad, A. Ziv, Z. Nevo and P. Mishra, "Cost-effective analysis of post-silicon functional coverage events," in *Design Automation and Test in Europe (DATE)*, pages 392-397, Lausanne, Switzerland, March 27 - 31, 2017.
6. **F. Farahmandi**, Y. Huang and P. Mishra, "Trojan Localization using Symbolic Algebra," in *Asia and South Pacific Design Automation Conference (ASPDAC)*, pages 591-597, Tokyo, Japan, January 16 - 19, 2017. **Best paper nomination**
7. **F. Farahmandi**, and P. Mishra, "FSM Anomaly Detection using Formal Analysis," in *IEEE International Conference on Computer Design (ICCD)*, pages 313-320, Boston, United States, November 5 - 8, 2017.
8. **F. Farahmandi** and P. Mishra, "Automated Test Generation for Debugging Arithmetic Circuits," in *Design Automation and Test in Europe (DATE)*, pages 1351-1356, Dresden, Germany, March 14 - 18, 2016.
9. **F. Farahmandi**, S. Ray and P. Mishra, "Exploiting Transaction Level Models for Observability-aware Post-silicon Test Generation," in *Design Automation and Test in Europe (DATE)*, pages 1477-1480, Dresden, Germany, March 14 - 18, 2016.
10. X. Guo, R. G. Dutta, Y. Jin, **F. Farahmandi** and P. Mishra, "Pre-Silicon Security Verification and Validation: A Formal Perspective," in *ACM/IEEE Design Automation Conference (DAC)*, pages 145:1-145:6, San Francisco, USA., June 7 - 11, 2015.
11. **F. Farahmandi**, B. Alizadeh and Z. Navabi. "Effective Combination of Algebraic Techniques and Decision Diagrams to Formally Verify Large Arithmetic Circuits," in *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 338-343, Tampa, USA, July 9 - 11, 2014.
12. S. Sadeghi Kohan, S. Keshavarz, F. Zokaee, **F. Farahmandi**, and Z. Navabi. "A new structure for interconnect offline testing," in *East-West Design and Test Symposium (EWDTS)*, pages 1-5, Rostov-on-Don, Russia, September 27-30, 2013.

Posters Presentations

1. "Formal Verification of Hardware Security and Trust," in *Design Automation Conference*, San Francisco, CA, 2018.
2. "IPTrust: Validation of IP Security and Trust," in *ACM Capital Region Celebration of Women in Computing*, Washington, D.C., 2017.
3. "IP Trust Validation using Formal Methods," in *FICS Annual Conference on Cybersecurity*, Gainesville, FL, 2017.
4. "Hardware Trojan Localization using Polynomials," in *ACM/IEEE Design Automation Conference*, Austin, TX, 2016.

5. "Observability-aware Post-Silicon Test Generation," in *Computing Research Association-Women (CRA-W) Grad Cohort*, San Diego, CA, 2016.
6. "Trust Validation of Hardware Intellectual Property (IP) Cores," in *FICS Annual Conference on Cybersecurity*, Gainesville, FL, 2016.
7. "Formal Verification of Arithmetic Circuits based on Symbolic Computer Algebra," in *Design Automation Conference*, San Francisco, CA, 2015.
8. "A Low-Power Enhanced Bitmask-Dictionary Scheme for Test Data Compression", in *IEEE Computer Society Annual Symposium on VLSI*, Tampa, FL, 2014.

Oral Presentations

ECE Department at Northeastern University,Boston, MA March 2018
IoT Devices: Challenges and Countermeasures

IEEE International Conference on Computer Design, Boston, MA November 2017
Feature-based Signal Selection for Post-silicon Debug using Machine Learning

IEEE Computer Society Annual Symposium on VLSI, Tampa, FL July 2014
Layout-aware Selection of Trace Signals for Post-Silicon Debug

Microprocessor/SoC Test and Verification Austin, TX December 2013
Dynamic Selection of Trace Signals for Post-Silicon Debug

Research Projects

1. **Vulnerability Identification in Controller Designs:** developed a framework based on symbolic algebra to detect and mitigate vulnerabilities in finite state machines against fault injection and hardware Trojan insertion attacks. The framework detects unauthorized accesses to the protected states of SoC controller designs. This project is funded by Cisco Systems.
2. **Post-silicon Test Generation for SoCs:** implemented a scalable directed test generation approach for RTL and gate-level designs by effective utilization of constraint solvers, automatic test pattern generation, symbolic algebra, and concrete simulation. This project is funded by Semiconductor Research Corporation (SRC) and National Science Foundation (NSF).
3. **Analysis of Post-Silicon Functional Coverage** developed signal selection algorithms and utilized on-chip design-for-debug infrastructure (trace buffers, scan chains) to perform post-silicon functional coverage analysis to reduce required synthesized coverage monitors. This project is funded by IBM.
4. **IP Integrity Validation using Formal Analysis:** designed a method that formally analyzes hardware designs and detects malicious components in third-party intellectual properties. The framework effectively utilizes polynomial models in order to address the scalability issues of the existing approaches. This project is funded by Semiconductor Research Corporation (SRC) and National Science Foundation (NSF).
5. **Automated Debugging of Arithmetic Circuit:** performed equivalence checking, automated test generation, bug localization and bug detection for arithmetic circuits using graph representation of the gate-level netlist and extracting polynomial models of the design's specification and its implementation.
6. **SoC Validation using Transaction Level Models:** implemented a scalable observability-friendly test generation technique using SystemC description of the design and bounded model checking which consists of assertion mapping, time mapping and test translation steps. This project was funded by Semiconductor Research Corporation (SRC) and National Science Foundation (NSF).

Teaching Experience

1. **University of Florida**, Gainesville, FL
   Teaching Assistant for Embedded Systems Spring 2018
   -Held office hours, designed homework and exam questions, graded homework, exam questions and computer assignments

   Teaching Assistant for Introduction to Computer Organization Fall 2013, Fall 2016
   -Gave lectures for two classes (70+ students), Held office hours, designed homework and exam questions, graded homework, exam questions and computer assignments

   Teaching Assistant for Data Structure and Algorithms Spring 2014
   -Held office hours, designed computer assignments and exam questions, graded exam questions and computer assignments, mentored student projects

2. **University of Illinois at Chicago**, Chicago, IL
   Chief Teaching Assistant for Advanced Computer Architecture Fall 2012
   -Held online office hours, designed computer assignments and exam questions, graded exam questions and computer assignments

3. **University of Tehran**, Tehran, Iran
   Teaching Assistant for Electronic System Level Design Methodology — Spring 2013
   -Prepared course lectures, designed homework and exam questions, graded exam questions and computer assignments, regular updates on students' projects

   Instructor for Digital Logic Design Laboratory — Fall 2011, Spring 2012, Fall 2012 and Spring 2013
   -Taught design practices using FPGAs (20+ students), prepared syllabus, designing computer assignments and graded exam questions and computer assignments, prepared lab sheets

   Teaching Assistant for Digital Logic Design — Spring 2007, Fall 2010, Fall 2008, Spring 2011 and Spring 2012
   -Graded homework, exam questions and computer assignments

   Teaching Assistant for Discrete Mathematics — Fall 2008 and Spring 2009
   -Graded homework and computer assignments

Professional Activities and Services

Associate Editor

1. IET Computers Digital Techniques (CDT)

Conference Program Committee

1. Technical Program Committee, International Conference on VLSI Design, 2019.
2. Technical Program Committee, International Conference on Embedded Systems, 2019.

Peer Reviewing

1. ACM/IEEE Design Automation and Test in Europe, 2014
2. ACM/IEEE, Design Automation Conference, 2015, 2018 and 2019
3. International Conference on Hardware/Software Codesign and System Synthesis, 2015 and 2018
4. IET Computers and Digital Techniques, 2015
5. IEEE Transactions on Very Large Scale Integration, 2016 and 2018
6. ACM Transactions on Design Automation of Electronic Systems, 2016 and 2017
7. IEEE International Symposium on Hardware Oriented Security and Trust, 2018
8. International Conference On Computer Aided Design, 2018
9. IEEE Asian Hardware Oriented Security and Trust Symposium, 2018
10. Journal of Hardware and Systems Security, 2019
11. Journal of Electronic Testing: Theory and Applications, 2019

Proposal Writing Experience

1. IPTrust: A Comprehensive Framework for IP Integrity Validation, funded by Semiconductor Research Corporation (SRC) and National Science Foundation (NSF)
   -Contribution: Writing draft for the PIs regarding our proposed equivalence checking framework.
2. Verification of IP Trust: A scalable framework for IP trust verification through formal methods, funded by Cisco Systems
   -Contribution: Writing draft for the PIs regarding proposed automatic hardware Trojan locating using symbolic algebra and security properties.

Membership

1. Institute of Electrical and Electronics Engineers (IEEE)
   - IEEE Women for Engineering and IEEE Young Professionals
2. Association for Computing Machinery (ACM)

Leadership Experience

1. Office holder (secretary) in Iranian Student Association (ISA) at the University of Florida — Fall 2015 -Summer 2016
   - Managing a cultural group with more than 200 members

Collaborators

1. Prof. Mark Tehranipoor, Ph.D., University of Florida, Gainesville, FL, USA
2. Prof. Yier Jin, Ph.D., University of Florida, Gainesville, FL, USA
3. Prof. Domenic Forte, Ph.D., University of Florida, Gainesville, FL, USA
4. Prof. Sandip Ray, Ph.D., University of Florida, Gainesville, FL, USA
5. Avi Ziv, Ph.D., IBM, Haifa, Israel

6. Ronny Morad, M.Sc, IBM Research, Haifa, Israel
7. Ziv Nevo, M.Sc, IBM Research, Haifa, Israel
8. Yousef Iskander, Ph.D., Cisco, Knoxville, TN, USA

Mentorship Experience

I have mentored seven undergraduates and one graduate student at the University of Florida.

1. Alif Ahmed, graduate student — Fall 2016-present
2. Jonathan Cruz, undergraduate student — Fall 2016-Summer 2017
3. James Safko, undergraduate student — Spring 2017
4. John Barta, undergraduate student — Spring 2017
5. Ryan Blanchard, undergraduate student — Spring 2016-Fall 2016
6. Timon Angerhofer, undergraduate student — Fall 2016
7. Emre Ozgener, undergraduate student — Spring 2015-Spring 2016
8. Rachel Johnson, undergraduate student — Fall 2014-Summer 2015

Technical Skills

Languages: C/C++, Java, Python, Verilog, VHDL, SystemC, SystemVerilog, batch programming, MATLAB, Octave, SQL, HTML, CUDA, Assembly, openCL
Tools: Xilinx ISE, ModelSim, SimpleScalar, Cadence and Synopsys design tools (HSPICE, Design Compiler, IC Compiler, VCS, Formality, Tetramax ATPG, Prime Time), Eclipse
Verification Tools: SMV model checker, VIS, ABC, Singular, minisat, Z3 SMT Solver
Others: MySQL, Oracle, SQLite, LaTeX, Django, Bootstrap, Redhat (Linux), Git

References

Prabhat Mishra, Ph.D.
UF Term Professor
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Priyank Kalla, Ph.D.
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